Claims amended After Final

AMENDMENT

In the Claims:

This listing of claim replaces all prior versions, and listings, of claims in the application:

1-5. (Cancelled)

6. (Currently Amended) A method of manufacturing an insulated gate semiconductor device, comprising:

forming a first gate oxide film on a semiconductor substrate of a first conductivity type;

forming a first silicon layer on the first gate oxide film;

forming an oxidation protection film having a predetermined pattern on the first silicon layer;

forming a field oxidation film and a second gate oxide film through selective oxidation by using the oxidation protection film as a mask, the second gate oxide film being in contact with the first gate oxide film;

forming a second silicon layer covering the first silicon layer remaining after the selective oxidation, the second gate oxide film and the field oxidation film after removing the oxidation protection film;

isolating a portion of the second silicon layer by etching so that the isolated portion of the second silicon layer covers at least part of the second gate oxide film and a portion of the remaining first silicon layer; and

forming a source layer or a drain layer which is of a second conductivity type,

wherein the formation of the field oxidation film and the second gate oxide film is performed after the formation of the first silicon layer, and the formation of the second silicon layer is performed after the formation of the field oxidation film and the second gate oxide film.

7. (Currently Amended) A method of manufacturing an insulated gate semiconductor device, comprising:

forming a low impurity concentration source layer and a low impurity concentration drain layer which are of a second conductivity type in a semiconductor substrate of a first conductivity type;

forming a first gate oxide film on the semiconductor substrate;

forming a first silicon layer on the first gate oxide film;

forming an oxidation protection film having a predetermined pattern on the first silicon layer;

forming a field oxidation film and a second gate oxide film through selective oxidation by using the oxidation protection film as a mask, the second gate oxide film being in contact with the first gate oxide film;

forming a second silicon layer covering the first silicon layer remaining after the selective oxidation, the second gate oxide film and the field oxidation film after removing the oxidation protection film;

isolating a portion of the second silicon layer by etching so that the isolated portion of the second silicon layer is positioned between the low impurity concentration source and drain layers and covers the remaining first silicon layer and at least part of the second gate oxide film; and

forming a high impurity concentration source layer of the second conductivity type in the low impurity concentration source layer and forming a high impurity concentration drain layer of the second conductivity type in the low impurity concentration drain layer,

wherein the formation of the field oxidation film and the second gate oxide film is performed after the formation of the first silicon layer, and the formation of the second silicon layer is performed after the formation of the field oxidation film and the second gate oxide film.

8. (Previously Presented) The method of manufacturing an insulated gate semiconductor device of claim 7, wherein the first and second silicon layers comprise polysilicon or amorphous silicon.

9. (Previously Presented) The method of manufacturing an insulated gate semiconductor device of claim 7, wherein the oxidation protection film comprises silicon nitride.

10. (Previously Presented) The method of manufacturing an insulated gate semiconductor device of claim 6, wherein the first and second silicon layers comprise polysilicon or amorphous silicon.

11. (Previously Presented) The method of manufacturing an insulated gate semiconductor device of claim 6, wherein the oxidation protection film comprises silicon nitride.

Claims on which Final Rejection

In the Claims:

1-5. (Cancelled)

6. (Currently Amended) A ~~manufacturing~~ method of manufacturing an insulated gate semiconductor device, comprising:

forming a first gate oxide film on a semiconductor substrate of a first conductivity type;

forming a first silicon layer ~~and~~ on the first gate oxide film;

forming an oxidation protection film having a predetermined pattern on ~~top of~~ the first silicon layer ~~on a predetermined area of the first gate oxide film~~;

forming a field oxidation film and a second gate oxide film through selective oxidation by using the oxidation protection film as a mask, the second gate oxide film being in contact with the first gate oxide film;

forming a second silicon layer covering ~~an entire area of a device intermediate~~ the first silicon layer remaining after the selective oxidation, the second gate oxide film and the field oxidation film after removing the oxidation protection film;

~~forming a gate electrode comprising the first silicon layer remaining on the first gate oxide film and~~ isolating a portion of the second silicon layer by etching ~~superimposed on the first silicon layer and partially extending over~~ so that the isolated portion of the second silicon layer covers at least part of the second gate oxide film and a portion of the remaining first silicon layer; and

forming a source layer [[and]] or a drain ~~layers~~ layer which is of a second conductivity type ~~away from the gate electrode~~.

7. (Currently Amended) A ~~manufacturing~~ method of manufacturing an insulated gate semiconductor device, comprising:

forming a low impurity concentration source layer and a low impurity concentration drain ~~layers~~ layer which are of a second conductivity type [[on]] in a semiconductor substrate of a ~~second~~ first conductivity type;

forming a first gate oxide film on the semiconductor substrate;

forming a first silicon layer ~~and~~ on the first gate oxide film;

forming an oxidation protection film having a predetermined pattern on ~~top of~~ the first silicon layer ~~on a predetermined area of the first gate oxide film~~;

forming a field oxidation film and a second gate oxide film through selective oxidation by using the oxidation protection film as a mask, the second gate oxide film being in contact with the first gate oxide film;

forming a second silicon layer covering ~~an entire area of a device intermediate~~ the first silicon layer remaining after the selective oxidation, the second gate oxide film and the field oxidation film after removing the oxidation protection film;

~~forming a gate electrode comprising the first silicon layer remaining on the first gate oxide film and~~ isolating a portion of the second silicon layer by etching ~~superimposed on the first silicon layer and partially extending over~~ so that the isolated portion of the second silicon layer is positioned between the low impurity concentration source and drain layers and covers the remaining first silicon layer and at least part of the second gate oxide film; and

forming a high impurity concentration source layer of the second conductivity type in the low impurity concentration source layer and forming a high impurity concentration drain ~~layers~~

layer of the second conductivity type in the low impurity concentration drain layer ~~away from the gate electrode~~.

8. (Currently Amended) The ~~manufacturing~~ method of [[the]] manufacturing an insulated gate semiconductor device of claim [[6 or]] 7, wherein the first and second silicon layers comprise polysilicon or amorphous silicon.

9. (Currently Amended) The ~~manufacturing~~ method of [[the]] manufacturing an insulated gate semiconductor device of claim [[6 or]] 7, wherein the oxidation protection film comprises silicon nitride.

10. (New) The method of manufacturing an insulated gate semiconductor device of claim 6, wherein the first and second silicon layers comprise polysilicon or amorphous silicon.

11. (New) The method of manufacturing an insulated gate semiconductor device of claim 6, wherein the oxidation protection film comprises silicon nitride.